

University of Bahrain
College of Information technology
Department of Computer Engineering

Test (1)

Student Name	
I.D. No.	
Section	

Course Title: Digital Logic

Course number: ITCE 202

Semester: 2

Academic Year: 2008/2009

Duration : 1 hour 15 minutes

Date: 27th April 2009

Read the following before you start:

1. Write your name, ID and section number
2. Answer all questions.
3. Write your answers on the attached sheets only.

Question	Mark	Mark attained
1	30	
2	20	
3	20	
4	30	
Total	100	

Question [1]: [30 mark]

a. Convert the following numbers showing all steps.

[4 marks each]

$$(D38.5)_{16} = (\quad)_4$$

$$(0011\ 0010)_{BCD} = (\quad)_{\text{excess-3}}$$

$$(6)_{10} = (\quad)_{7-4-4-1}$$

$$(100010010100)_{2's\ complement} = (\quad)_{1's\ complement}$$

$$(-15)_{10} = (\quad)_{2's\ complement}$$

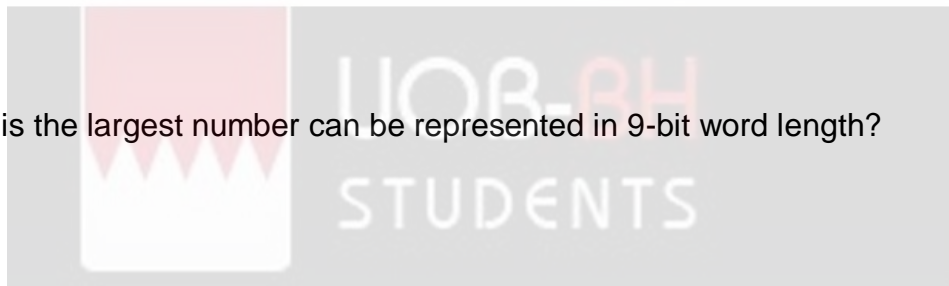
$$(+15)_{10} = (\quad)_{1's\ complement}$$

b. Add the following 2's complement numbers and indicate if over flow occur. [4 marks]

$$\begin{array}{r} 1\ 1\ 1\ 1\ 0\ 1\ 1 \\ +1\ 0\ 0\ 0\ 1\ 1\ 1 \\ \hline \end{array}$$

c. What is the largest number can be represented in 9-bit word length?

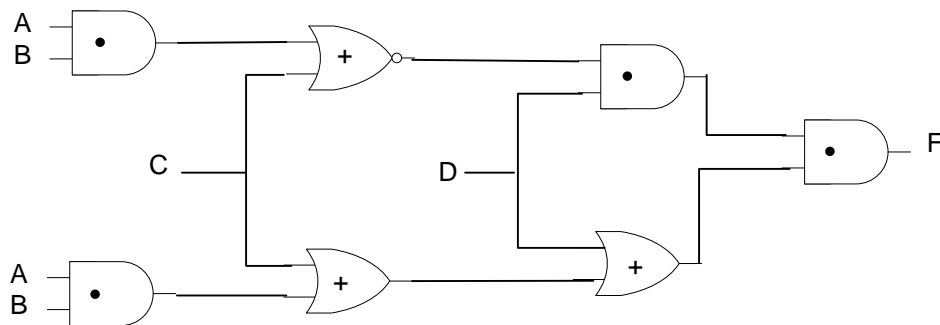
[2 marks]



Question [2] : [20 mark]

- a. Find and simplify the Boolean expression of the following logic circuit.
b. How many level the circuit consist of ?

[12 mark]



- c. Apply DeMorgan's Law directly on the following expression to find Z' , do not simplify.

[8 marks]

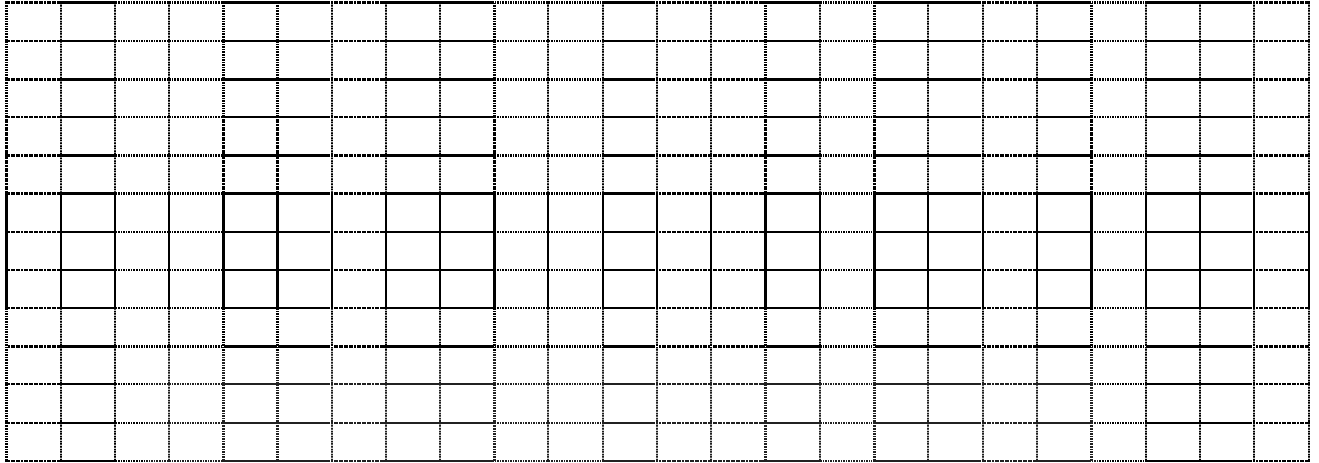
$$Z = \left((A \oplus B)' + (CD + F)A' \right) D + (A \oplus B')$$



Question [3]: [20 mark]

a. Design a minimum three-level circuit to realize the following Boolean function using all NOR gate circuit. Draw the circuit. Do not use inverter at output.

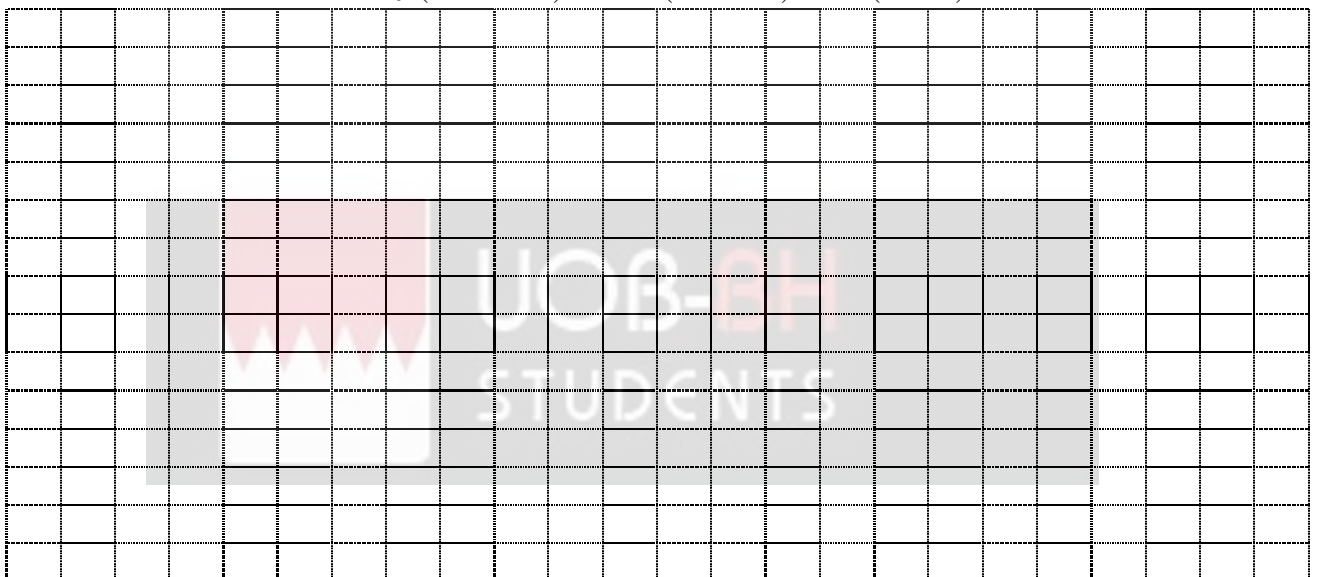
$$f(A, B, C, D) = \bar{A}B + A\bar{D} + A\bar{B}\bar{C}$$



b. Repeat part (a) using 4-level all NOR circuit.

c. Design a minimum logic circuit to realize the following Boolean function using all NAND gate circuit.(maximum of 3-input NAND gates)

$$f(A, B, C, D) = \Pi M(3, 8, 10, 15) \bullet \Pi D(2, 5, 12)$$



- b.** Find the Minterm expansion of segment c in decimal notation.
- c.** Find the Maxterm expansion of segment d' in decimal notation.
- d.** Draw a minimum logic circuit for segment a using NAND gates only.
- e.** Find the minimum sum of products for segment b.
- f.** Show how you can make the circuit for segment d using an XOR gate in your design.

